Nanoengineered Curie Temperature in Laterally-patterned Ferromagnetic Semiconductor Heterostructures

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We demonstrate the manipulation of the Curie temperature of buried layers of the ferromagnetic semiconductor (Ga,Mn)As using nanolithography to enhance the effect of annealing. Patterning the GaAs-capped ferromagnetic layers into nanowires exposes free surfaces at the sidewalls of the patterned (Ga,Mn)As layers and thus allows the removal of Mn interstitials using annealing. This leads to an enhanced Curie temperature and reduced resistivity compared to unpatterned samples. For a fixed annealing time, the enhancement of the Curie temperature is larger for narrower nanowires.

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Heterostructures derived from the ferromagnetic semiconductor (Ga,Mn)As are important for studying spin-dependent device concepts[1,2,3,4,5] relevant to semiconductor spintronics.[6,7,8] In contrast to metallic ferromagnets where crystalline defects rarely affect the magnetic ordering temperature, it is now well established that Mn interstitial defects – double donors that compensate holes – play a key role in limiting the hole-mediated Curie temperature (T_C) of (Ga,Mn)As to below 110 K in as-grown samples.[9] In thin (Ga,Mn)As epitaxial layers, post-growth annealing[10,11] drives Mn interstitials to benign regions at the free surface where they are passivated, resulting in significant increases in both the hole density (p) and T_C (which can be as high as 160 K).[12,13,14] Such values of T_C should in principle allow the fabrication of proof-of-concept spintronic devices operating above liquid nitrogen temperatures. Unfortunately, the annealing-induced enhancement of T_C is almost completely suppressed in heterostructure devices containing buried (Ga,Mn)As layers.[15,16] In this Letter, we describe a nanoengineered solution to this problem: lithographic patterning of (Ga,Mn)As heterostructures into nanowires. Such patterning opens up new pathways for defect diffusion to free surfaces at the sidewalls, and thus restores the annealing-enhanced T_C to buried (Ga,Mn)As layers. These results suggest novel routes towards the flexible fabrication of (Ga,Mn)As-based spintronic devices with relatively high T_C.

Laterally-patterned wires are fabricated from GaAs/(Ga,Mn)As/GaAs heterostructures grown by molecular beam epitaxy on epiready semi-insulating GaAs (100) substrates. Crystal growth conditions are identical to those described in an earlier publication.[15] The samples consist of a 5 nm thick low temperature GaAs buffer layer, followed by a (Ga,Mn)As layer ($\sim$ 6%Mn, thickness of 15 nm or 50 nm) and finally a low temperature grown 10 nm GaAs capping layer. The data shown are for 50 nm thick magnetic layers, but the results were qualitatively the same for the 15 nm thick samples. We pattern these samples into wires that are approximately 4 μm long and with two different widths (1 μm and 70 nm) using electron beam lithography followed by lift off and dry etching.

For the patterning process, the samples are first spin coated with a bilayer of about 400-nm-thick electron-beam resist P(MMA-MAA) copolymer/PMMA with molecular weight of 950. The desired patterns are defined on the sample using direct-write electron-beam lithography at electron energy of 100 keV. After development of the resist in MIBK:IPA 1:1 solution, a metallic layer of either 45 nm Al or Al/Au is deposited on the sample using thermal evaporation. Using standard lift off techniques, we then obtain metal wires that serve as a hard mask for the subsequent chlorine-based dry etching process. After dry etching, for samples with an Al mask, the metal layer is dissolved in CD-26 photoresist developer, leaving just the semiconductor nanowire; for samples with an Al/Au mask, the metal is retained on portions of the sample. We note that in the latter case the undoped GaAs capping layer serves as an insulator that prevents the shunting of current through the metal during the measurement.[17] Figures 1 (a) and (b) show plan view SEM images of patterned nanowires. Three identical rows of wires are patterned on each wafer: one set is measured as-grown and patterned, while the other two sets are annealed after patterning at 190°C for 5 hours.

We probe the ferromagnetic phase transition in single wires using four probe measurements of the temperature-dependent resistivity $\rho(T)$; it is well-established[7,8] that $\rho(T)$ shows a well-defined peak close to T_C in (Ga,Mn)As, especially for samples with $T_C < 100$ K. For higher T_C, the peak is less well-defined but still yields a reasonable estimate of the ordering temperature (typically an overestimate of $\sim$ 10K). In addition, we measure the temperature-dependence of both the magnetization (using a commercial superconducting quantum interference device (SQUID) magnetometer) and the resistivity in macroscopic pieces of the parent wafers (using the van der Pauw method).

Figure 2 (a) shows the magnetization as a function of temperature for both as-grown and annealed ($\sim$ 5mm^2) pieces of a GaAs/50 nm (Ga,Mn)As/10 nm GaAs heterostructure. As found in earlier studies,[15] the cap layer

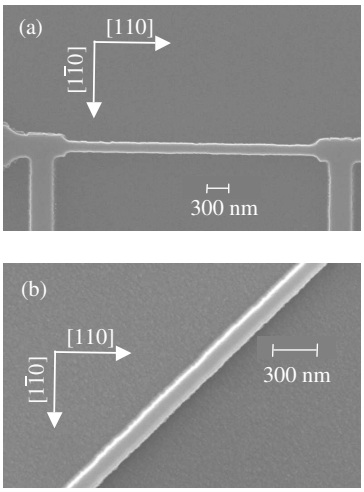

FIG. 1: SEM images of nanowires patterned along two different crystallographic directions: (a) [110] and (b) [010].

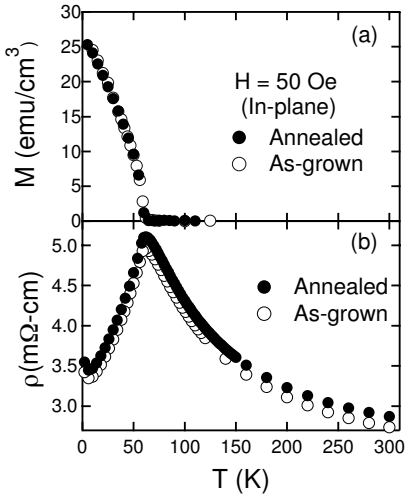

FIG. 2: (a) Magnetization versus temperature for macroscopic pieces (area of $\sim$ 5mm^2) of as-grown and annealed GaAs/(Ga,Mn)As (50 nm)/ (10 nm) GaAs heterostructure. The data are measured in a magnetic field of 50 Oe in-plane upon warming after field cooling at 10 kOe. The sample is annealed at 190°C in ultrahigh purity nitrogen gas (5N) for 5 hours. The data show that T_C is not affected by annealing. (b) Resistivity versus temperature (measured in van der Pauw geometry) for a 1 mm $\times$ 2 mm mesa patterned from the same wafer as in (a).

completely suppresses any annealing-induced enhancement of T_C. This suppression of the annealing effect has been attributed to the formation of a p-n junction at each of the two GaAs/(Ga,Mn)As interfaces as some Mn interstitials (double donors) initially diffuse across the boundaries into GaAs.[14,15] The resulting Coulomb barrier is expected to strongly inhibit the further diffusion of Mn interstitials from the bulk of the (Ga,Mn)As layer towards the interfaces. The temperature-dependence of the sample resistance is in complete agreement with the magnetization measurements. Figure 2(b) shows Van der Pauw measurements of $\rho(T)$ for a macroscopic mesa (1mm $\times$ 2mm); the peak of $\rho(T)$ does not change upon annealing. In addition, there is no significant reduction in the resistivity of the sample with annealing, indicating that the hole density has not changed.

Lateral patterning produces distinctly different behavior. Figure 3(a) shows the temperature-dependent resistivity for a 1μm wide wire patterned along the [110] direction. The data are shown for both an as-grown wire and one annealed at 190°C for five hours. The data indicate that annealing results in a slight increase in T_C, accompanied by a slight increase in the resistivity of the sample. These observations suggest that annealing induces modest diffusion of Mn interstitials to the free surfaces at the sidewalls of the wire. The diffusion coefficient (estimated to be $D \sim 100$nm^2/hr at ~ 190°C[14]) is simply not large enough to allow significant removal of Mn interstitials from the bulk of the 1μm wide wire within the five hours annealing time. There is however some alteration of the defect states, as indicated by the small increase in the high temperature resistivity; we do not have an explanation for this observation but note that a similar effect has been seen in previous studies of long anneals, albeit at higher annealing temperatures.[11] Figure 3 (b) shows the effect of annealing for a 70 nm wide nanowire (also patterned along [110]). Here, annealing produces a striking increase in T_C of almost 50 K, accompanied by a correspondingly significant decrease in the resistivity of the wire. Both these observations strongly suggest the successful removal of the Mn interstitials from the bulk of the (Ga,Mn)As nanowire. Lateral diffusion of the Mn interstitials provides the most likely explanation for these observations. We note that the time and length scales for diffusion observed in our experiments ($\sim$ 35 nm in 5 hours) are consistent with earlier low-temperature annealing studies of (Ga,Mn)As epilayers.[14]

It is important to examine whether defect-diffusion may depend on the crystalline direction and/or the nature of the free surface where the interstitials eventually reside. We hence pattern four nanowires (each with 70 nm width), along the principal cubic directions ([110],[100],[1$\bar{1}$0] and [010]). All four nanowires are annealed under identical conditions (190°C for 5 hours). The results are shown in Fig. 3(c) and indicate that at least for the processing and annealing protocol followed in this study defect diffusion does not vary significantly with crystalline direction.

In summary, we have shown that nanolithography allows the engineering of defect diffusion pathways, hence

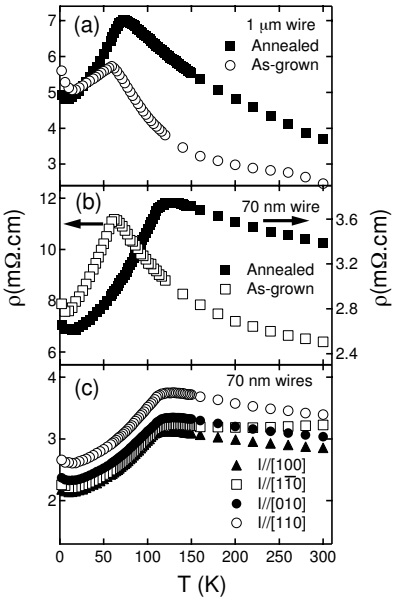

FIG. 3: Temperature dependence of the (four-probe) resistivity for as-grown and annealed single wires of (a) 1 micron width and (b) 70 nm width. Both sets of wires are patterned along the [110] direction. Plot (c) shows the same measurements for four individual 70 nm wires patterned along different crystalline orientations. All wires are patterned from the same wafer used in Fig. 2, and the annealing conditions are identical to those used in Fig. 2.

providing a means of tailoring impurity-controlled magnetism in ferromagnetic semiconductor heterostructures. Areas with different T_C and resistivity can be made on the same wafer simply by having different feature sizes. Smaller features have a higher Curie temperature and lower resistivity. Although we do not observe any obvious crystalline anisotropy in the diffusion constant of the Mn interstitials, such directional dependence may still exist and may be revealed by in situ resistance monitoring while annealing the nanowires. Our findings augur well for prospects of designing (Ga,Mn)As-based spintronic device heterostructures such as magnetic tunnel junctions with T_C well above 77 K. In addition, systematic studies of annealing of nanowires of differing width may provide new insights into ongoing controversies about the microscopic details of the diffusion and passivation of Mn interstitials in (Ga,Mn)As.[18]

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